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verse directions in said semiconductor substrate, said semiconductor pillar projections being arranged in a matrix manner;
a plurality of HOS capacitors formed on side surfaces at a lower portion of each of said semiconductor pillar projections, said each HOS capacitor including:
a memory node formed in side surface at the lower portion of each semiconductor pillar projection,
a capacitor insulating film formed on the side surface at the lower portion of each semiconductor pillar projection, and
a capacitor electrode formed on said capacitor insulating film;
a plurality of MOSFETs formed on side surfaces at an upper portion of each semiconductor pillar projection, said seach MOSFET including,
a channel region formed at least on the side surface of the upper portion of each semiconductor pillar projection,
source and drain regions formed above and below said channel region to sandwich said channel region,
a gate insulating film formed on the side surface at the upper portion of each semiconductor pillar projection in which said channel region is formed, and
a gate electrode formed on said gate insulating film;
a plurality of bit line contacts each contact formed on an upper surface of a corresponding semiconductor pillar projection; and
a plurality of bit lines each bit line connected to associated bit line contacts;

wherein said plurality of semiconductor pillar projections is divided into a plurality of blocks, each block having at least one contact semiconductor pillar projection comprising a first insulating layer which is thicker than said gate insulating film of said MOSFET and is formed on an upper surface of said contact semiconductor pillar projection, and a word line contact pad formed on said first insulating layer, said contact pad being electrically connected to said gate electrode of memory cells in each block.

A step can be formed in the middle of the side surfaces of the pillar projection, a diffusion layer serving as a memory node is formed on side surfaces at a lower portion of the step, and a capacitor electrode is formed on the side surfaces at the lower portion with a capacitor insulating film interposed therebetween.

Since each memory is formed on the side surfaces of the pillar projection and α-rays incident obliquely are interrupted by an array of the pillar projections, a soft error in a cell mode can be similarly suppressed. Furthermore, a step is formed on the side surfaces of the pillar projection by the two-step groove formation using first and second masks, and the diffusion layer serving as a memory node is formed in side surfaces at a lower portion of the step. Therefore, a DRAM cell having excellent characteristics can be obtained.

Other objects and advantages will be apparent from the following description taken in conjunction with the accompanying drawings, in which:

Fig. 1 is a plan view showing a DRAM useful for understanding the present invention;
Fig. 2A is a sectional view taken along a line IIA - IIA in Fig. 1;
Fig. 2B is a sectional view taken along a line IIB - IIB in Fig. 1;
Figs. 3A to 3I are sectional views showing a method of manufacturing the DRAM of Fig. 1;
Fig. 4 is a plan view showing a DRAM of a folded bit line type;
Figs. 5A to 5E are sectional views showing another method of manufacturing a DRAM useful for understanding the present invention;
Figs. 6A and 6B are sectional views showing a method of manufacturing a DRAM having a height of a gate electrode different from that of a gate electrode of the device shown in Fig. 1;
Figs. 7A and 7B are sectional views showing a method of manufacturing a DRAM capable of preventing a step from being formed on side surfaces of a pillar projection;
Figs. 8A to 8C are sectional views showing a method of manufacturing a DRAM capable of improving element isolation;
Figs. 9A and 9B are sectional views showing a method of manufacturing a DRAM capable of improving element isolation;
Fig. 10A is a plan view showing a DRAM in which a word line can be patterned without a photolithograpic step;
Fig. 10B is a sectional view taken along a line XB - XB in Fig. 10A;
Figs. 11A and 11B are plan views for explaining a manufacturing method for connecting a word line without a photolithograpic step;
Figs. 12A and 12B are sectional views showing still another modification of a DRAM manufacturing method for connecting a word line without a photolithographic step;
Figs. 13A to 13F are sectional views for explaining a DRAM manufacturing method using an isolating insulating film different from that in the method described with reference to Figs. 3A - 3I in order to insulatively isolate a capacitor electrode from a gate electrode;
Fig. 14A is a plan view showing another DRAM useful for understanding the present invention;
Fig. 14B is a sectional view taken along a line XIVB - XIVB in Fig. 14A;
Figs. 15A to 15H are sectional views showing a method of manufacturing the DRAM shown in Figs. 14A and 14B;
Figs. 16A to 16E are sectional views showing a wa-

about 0.5 μm by RIE using the mask 25 to form third grooves 4c for isolating the layer 6 in units of memory cells. In this state, boron ions are implanted at an acceleration voltage of 100 keV and a dose of 5×10^{12} ions/cm^2 to form the p^+-type layer 9 as a channel stopper for assuring element isolation on a bottom portion of each groove 4c. Alternatively, a step of depositing the SiO_2 film 25 may be omitted, and the AsSG film 24 may be used as the third mask.

Thereafter, as shown in Fig. 3E, the film 25 is removed, and thermal oxidation is performed to form the 10-nm thick capacitor insulating film 7 on the side surfaces at the lower portion of the pillar projection 3. As the capacitor insulating film, a stacked film of an SiO_2 film and an Si_3N_4 film may be used, or a metal oxide film such as Ta_2O_5 or a thermal nitride film, or a combination of these films may be used.

As shown in Fig. 3F, the capacitor electrode 8 consisting of a first polycrystalline silicon film is buried in the groove 4. More specifically, a phosphorus-doped first polycrystalline silicon film is deposited to have a thickness of about 600 nm and etched by the CDE containing CF4 gas so that the surface of the electrode 8 is substantially leveled with the position of the step 5. In this example, a maximum width of the groove 4 is about 0.6 μm. Therefore, if the deposited polycrystalline silicon film has a thickness of about 0.3 μm or more, its surface is substantially flattened. The entire surface of the polycrystalline silicon film is etched by the CDE to bury the capacitor electrode 8 as shown in Fig. 3F. If the surface is not flattened even by depositing the polycrystalline silicon film, the surface is flattened by a fluid film such as a photoresist. In this case, the entire surface is etched so that etching rates for the fluid film and the polycrystalline silicon film are substantially equal to each other, thereby obtaining the structure shown in Fig. 3F. In this manner, a MOS capacitor utilizing the side surfaces at the lower portion of each pillar projection 3 not covered with the first and second masks 21 and 23 is formed.

Then, as shown in Fig. 3G, the Si_3N_4 film 23 and the underlying SiO_2 film 22 which cover the side surfaces at the upper portion of the projection 3 on which a MOSFET is to be formed are removed. Thereafter, thermal oxidation is performed in an $O_2 + HC\ell$ atmosphere at a temperature of 900°C for about 60 minutes, thereby forming the gate insulating film 11 on the side surfaces at the upper portion of the projection 3. At the same time, the SiO_2 film 10 having a film thickness two times that of the gate insulating film 11 is formed on the capacitor electrode 8. A phosphorus-doped second polycrystalline silicon film is then deposited to have a thickness of about 25 nm and etched by RIE, thereby forming the gate electrodes 12a and 12b on the side surfaces at the upper portions of the projections 3. Each gate electrodes 12a and 12b remain all around the projection 3 in a self-alignment manner without using a mask. The gate electrodes 12a and 12b must be continuously formed in one direction of the matrix to form word lines. For this purpose, a photoresist mask is formed on a region of grooves along the word line direction. In this manner, a MOSFET utilizing the side surfaces at the upper portion of the projection 3 is formed.

Thereafter, as shown in Fig. 3H, the surfaces of the gate electrodes 12a and 12b are covered with the SiO_2 film 13 formed by thermal oxidation, and the third polycrystalline silicon film 14 is buried in recess portions to flatten the overall substrate. The film 13 may be formed not by thermal oxidation but by CVD. In order to flatten the film 14, a polycrystalline silicon film is deposited on the entire surface, the surface is flattened by a photoresist, and the entire surfaces of the film and the photoresist are etched by dry etching performed at equal etching rate. Thereafter, thermal oxidation is performed in a vapor atmosphere at 850°C for about 10 minutes to form a SiO_2 film 26 on the surfaces of the gate electrodes 12a and 12b and the buried polycrystalline silicon film 14. At this time, the upper end face of each pillar projection 3 is covered with the Si_3N_4 film 21b as an anti-oxidation mask, and almost no SiO_2 film is formed.

As shown in Fig. 3I, the film 21b is etched by a gas containing, e.g., CF_4 gas, and As ions are implanted at a dose of 5×10^{12} ions/cm^2 and an acceleration voltage of 40 keV, thereby forming the n-type layer 16 serving as a source or drain of the MOSFET in the upper end face of the projection 3. At this time, if necessary, phosphorus ions may be implanted in the upper end face of the projection 3 at a dose of 3×10^{13} ions/cm^2 and an acceleration voltage of 100 keV to form an n^--type layer below the n-type layer 16, so that the MOSFET obtains an LDD structure. Thereafter, thermal oxidation is performed in a steam atmosphere at a temperature of 850°C to form the SiO_2 film 15 on the substrate surface. The thickness of the film 15 is about 40 nm on the surfaces of the gate electrode consisting of a polycrystalline silicon and the buried polycrystalline silicon film 14 and is about 10 nm on the upper end face of the projection 3. The SiO_2 film 15 is etched by an ammonium fluoride solution to selectively expose only the upper end face of each pillar projection 3. A W film is deposited and patterned to form the bit lines 17 connected to the n-type layer 16 and crossing the word lines. In this example, no PEP step is required for a bit line contact, and only the upper end face of the pillar projection 3 can be exposed in a self-alignment manner.

The DRAM according to this example has the following features. That is, the bit line is connected to the source or drain of the MOSFET in a self-alignment manner without a contact hole formation step including photolithography. Therefore, since an alignment margin required in the photolithography need not be formed, the size of the upper end face of each pillar projection is not limited by the alignment margin unlike in the conventional device. As a result, since the pillar projection can be minimized to a limit size, a memory cell can be micropatterned, and a high packing density and a large capacity of the DRAM can be realized. In addition, since

on the side surfaces of the pillar projection in the above example, but this step can be omitted. Figs. 7A and 7B show main steps of such a modification. As shown in Fig. 7A, an Si_3N_4 film 23 is formed on side surfaces of each pillar projection 3 obtained by forming a first groove, and a second groove 4b is formed by etching, as in the above example. Thereafter, as shown in Fig. 7B, the Si surface exposed in the second groove 4b is etched by dry etching containing CF4 gas to reduce a step. A MOS capacitor and a MOSFET are formed and a bit line is connected to the upper end face of the pillar projection in a self-alignment manner in the same manner as in the above example.

In this modification, even if an n^+-type layer serving as a memory node is diffused shallow, a corner does not extend into a channel region of the MOSFET because of the presence of the step. As a result, characteristics of the MOSFET can be improved.

Figs. 8A to 8C show main steps of a modification in which element isolation is performed more reliably. After second grooves 4b are formed via the step shown in Fig. 3B, boron ions, for example, are implanted at a dose of 3×10^{12} ions/cm^2 and 100 keV in bottom portions of the grooves 4b, thereby forming a p^+-type layer 9 serving as a channel stopper, as shown in Fig. 8A. At this time, ion implantation is performed vertically to a substrate. Thereafter, a CVD SiO_2 film 41 is deposited on the entire surface to have a film thickness of about 100 nm, and a fluid film such as a photoresist 42 is coated thereon to flatten a semiconductor structure. The film 42 is etched in an atmosphere containing O_2 gas so as to remain the film 42 only on a bottom portion of a groove by a thickness of about 0.5 μm.

As shown in Fig. 8B, the SiO2 film 41 is selectively etched by using the photoresist 42 as a mask and an ammonium fluoride solution so as to remain the SiO_2 film 41 only on a bottom portion of a groove 4. Thereafter, an arsenosilicate film (AsSG film) 43 containing arsenic as an impurity is deposited to have a thickness of about 70 nm. Annealing is performed in a nitrogen atmosphere at 1,000°C to diffuse As from the AsSG film 43, thereby forming an n^--type layer 6. At this time, since the thick SiO2 film 41 remains on the bottom portion of the groove, the n-type impurity is not diffused.

As shown in Fig. 8C, the film 43 is removed, a capacitor insulating film 7 is formed, and a capacitor electrode 8 consisting of a first polycrystalline silicon film is buried in the groove. Thereafter, a DRAM can be formed in accordance with the steps from Fig. 3G.

According to this modification, adjacent memory cells can be reliably isolated by the thick SiO_2 film 41 and the p-type layer 9. In addition, since the thick film 41 is formed, an impurity concentration of the layer 9 can be decreased. As a result, junction leakage between the n^--type layer 6 of the MOS capacitor and the p-type layer 9 can be reduced.

Figs. 9A and 9B show still another modification capable of obtaining the same effects as in the modification shown in Figs. 8A to 8C. After the SiO2 film 25 used as the third mask is removed in the step shown in Fig. 3D of the above example, a 70-nm thick CVD SiO2 film 51 is deposited on the entire surface, and a photoresist 52 is coated thereon to flatten a semiconductor structure. As shown in Fig. 9A, the photoresist 52 is etched by RIE in a gas atmosphere containing O_2 gas so as to remain the photoresist 52 on a bottom portion of a groove by a thickness of about 0.5 μm. As shown in Fig. 9B, the SiO_2 film 51 is selectively etched by, e.g., an ammonium fluoride solution by using the remaining photoresist 52 as a mask so as to remain the SiO_2 film 51 only on the bottom portion of the groove. Thereafter, the photoresist 52 is removed, a capacitor insulating film is formed, and a DRAM is manufactured in accordance with the steps from, e.g., Fig. 3F.

Also in this modification, adjacent memory cells can be reliably isolated. In addition, in this modification, the SiO_2 film 51 is caused to remain on the groove bottom portion after an n^--type layer is formed on a MOS capacitor region. Therefore, the film thickness of the film 51 is not much varied in the subsequent steps, thereby achieving element isolation with good uniformity.

A thick SiO_2 film for element isolation can be formed on a bottom of a groove by, e.g., selectively forming an Si_3N_4 film on side surfaces of the groove and oxidizing the semiconductor structure in a steam atmosphere. In this manner, an SiO_2 film having a thickness of about 70 nm can be formed on the groove bottom portion.

In the above modifications, in order to continuously form the gate electrode to be used as a word line, photolithography in which a mask of, e.g., a photoresist is formed between adjacent memory cells along a word line direction is used in the gate electrode patterning step. By considering a memory cell arrangement, however, the gate electrode also serving as a word line can be patterned without the photolithography using a photoresist. Such a modification will be described next.

Figs. 10A and 10B show a DRAM according to the such a modification. Referring to Figs. 10A and 10B, the same reference numerals as in the above example denote the same parts and a detailed description thereof will be omitted. A shown in Fig. 10A, pillar projections 3 for forming memory cells are arranged at an interval a in a word line direction and an interval b in a bit line direction. At this time, a value of the interval is set such that grooves are automatically buried upon deposition of a second polycrystalline silicon film 12 for forming gate electrodes also serving as word lines by, e.g., CVD. More specifically, the value of the interval a is set to be smaller than a value twice the film thickness of the second polycrystalline silicon film 12. For example, if the thickness of the film 12 is about 200 nm, the interval a is set to be 400 nm or less, e.g., 300 nm. A value of the interval b in the bit line direction is set to be larger than a value twice the thickness of the film 12. For example, if the thickness of the film 12 is 300 nm, the interval b is set to be 600 nm. With this pillar projection arrangement,

age property of a memory cell can be improved.

In the above modifications, in order to adjust a threshold value of the MOSFET, ions are implanted in the entire surface of the substrate to reach the MOSFET formation region before groove formation, thereby forming the p^--type layers. The p^--type layer, however, need only be formed in a side surface portion of each pillar projection serving as the MOSFET region. Therefore, for example, after the pillar projections are formed and the capacitors are buried, ion implantation may be performed to adjust an impurity concentration of a channel region. In this case, ion implantation is performed to the substantially vertical side surfaces. Therefore, by performing oblique ion implantation including rotation of the wafer, the impurity is uniformly doped in the side surfaces. In this case, the wafer may be continuously rotated or intermittently rotated every 90°.

Examples of the bit line material are, in addition to the W film or the Aℓ-Si-Cu film described in the above example, another refractory metal such as molybdenum, a refractory metal silicide, or a combination of these metals and a polycrystalline silicon film.

In the above example, the p-type Si substrate is used. The entire memory cell region, however, may be formed in a p-type well by, e.g., boron diffusion. At this time, if an impurity concentration of the groove bottom portion serving as an element isolation region is about 1×10^{17} atoms/cm^3, a p-type impurity diffusion step for element isolation can be omitted.

A second example useful for understanding the present invention will be described in detail below with reference to Figs. 14A and 14B.

Fig. 14A shows a four-bit DRAM portion.

Referring to Fig. 14A, a silicon oxide film 102 is formed on the surface of a p-type silicon substrate 101, and an n^--type layer 103 serving as a memory node of a MOS capacitor and a p^--type layer 104 serving as a channel region of a MOSFET are stacked thereon. A plurality of small pillar projections 105a, 105b, 105c and 105d isolated by grooves 106 formed in longitudinal and transverse directions in the substrate are arranged in a matrix manner.

A step 107 is formed on side surfaces of each pillar projection 105. A portion below a position slightly above the step 107 is the n^--type layer 103. A capacitor insulating film 108 is formed on all the side surfaces at a lower portion of the projection 105. A capacitor electrode 109 is buried in each groove 106. A MOS capacitor is constituted by the n^--type layer 103, the capacitor insulating film 108 and the capacitor electrode 109. A boundary between the n^--type layer 103 and the channel layer 104 is set to be a position equal to or slightly higher than that of the step 107. The capacitor electrode 109 is continuously formed as a plate electrode common for all memory cells. The electrode 109 is extracted at a peripheral portion of the DRAM.

The silicon oxide layer 102 is formed below bottom portions of the groove 106 and the projections 105. The layer 102 serves as an insulating layer for element isolation and for preventing a soft error caused by α-rays.

Gate electrodes 112a and 112b are formed on side surfaces at an upper portion of each pillar projection 105 with a gate insulating film 111 interposed therebetween. The gate electrode 112 and the capacitor electrode 109 are vertically buried in the groove 106 and isolated from each other by an insulating film 110. The gate electrodes 112 surround the projection 105 and are continuously formed in one direction of the matrix to serve as word lines. An insulating film 113 is buried in a recess portion of the groove 106 except for the buried gate electrode 112 to flatten a semiconductor structure.

The surface of the substrate in which the capacitor and gate electrodes 106 and 112 are buried is covered with the insulating film 113, and bit lines 117a and 117b consisting of, e.g., a polycide film of a polycrystalline silicon film doped with As and a tungsten silicide film are formed thereon. An n^+-type layer 116 serving as a source or drain of the MOSFET is diffused in the upper end face of each pillar projection 105. The bit line 117 is directly connected to the layer 116 in a self-alignment manner without performing a PEP step for forming a contact hole.

A method of manufacturing this DRAM will be described below.

As shown in Fig. 15A, the SiO_2 film 102 having a film thickness of about 8,000 Å is formed as an insulating film on the p-type silicon substrate 101, and the 3-μm thick n^--type layer 103 serving as a memory node is formed thereon by, e.g., thermal diffusion of antimony (Sb). The p^--type layer 104 serving as a channel region of the MOSFET is formed on the layer 104.

The substrate having the above layers is formed by, e.g., a method as shown in Figs. 16A to 16E. That is, a wafer bonding method will be described below with reference to Figs. 16A to 16E.

First, two wafers, i.e., silicon substrates 101 and 101S are prepared. As shown in Fig. 16A, boron (B) ions, for example, are implanted in the p^--type silicon substrate 101S at a dose of 5×10^{12} ions cm^{-2} and an acceleration voltage of 100 kev. The substrate 101S is annealed to form the p^--type layer 104 having a higher concentration than that of the substrate 101S. The p^--type layer is for forming a channel region of the MOSFET and is required to have a thickness of 6 μm or more and a uniform concentration region. The layer 104 may be formed by epitaxial growth in place of ion implantation. A thick layer having a uniform concentration can be easily formed by the epitaxial growth.

As shown in Fig. 16B, the n-type impurity layer 103 having a concentration of 1×10^{19} atoms cm^{-3} is formed on an arbitrary region of the substrate 101S to have a thickness of about 3 μm. The layer 103 can be formed by thermal diffusion of antimony (Sb) or the like or ion implantation of arsenic (As).

Oxide films 102a and 102b each having a thickness of 50 nm to 1 μm, e.g., 400 nm are formed on the sur-

about 20 nm.

As shown in Fig. 15F, a phosphorus-doped second polycrystalline silicon film is deposited to have a thickness of about 250 nm and etched by RIE, thereby forming the gate electrode 112 on the side surfaces at the upper portion of each pillar projection 105. The electrode 112 is formed in a self-alignment manner all around the projection 105 without a mask. The electrode 112 must be continuously formed in one direction of the matrix to form word lines. For this purpose, a photoresist mask is formed in a region of the groove along the word line direction. In this manner, the MOSFET is formed on the side surfaces at the upper portion of each pillar projection 105. If the projections 105 are arranged in the word line direction at a smaller interval than a direction perpendicular to the word line direction, connection portions can be formed in a self-alignment manner without a mask layer.

Thereafter, as shown in Fig. 15G, the surface of the gate electrode 112 is covered with the SiO_2 film 113 formed by thermal oxidation. A BPSG film 114, for example, is buried in the recess portion, and the entire substrate is flattened by annealing. The SiO_2 film 113 may be formed not by thermal oxidation but by CVD. The surface is flattened by a photoresist, and the SiO_2 film 113 and the BPSG film 14 are dry-etched at equal etching rates. As a result, the Si_3N_4 film 121b as an anti-oxidation mask present on the upper end face of the pillar projection 105 is exposed.

As shown in Fig. 15H, the film 121b is selectively etched by CDE using a gas containing CF_4 gas. Subsequently, the SiO_2 film 121a is removed to expose the Si substrate. Thereafter, thermal oxidation is performed in a steam atmosphere at a temperature of 850°C to form an SiO_2 film on the substrate surface. The thickness of the SiO_2 film is about 10 nm on the upper surface of the projection 105. If the thermal oxidation is performed while the upper end of the gate electrode is located above the upper surface of each projection 15, polycrystalline silicon portions after etching can be effectively connected to each other.

As ions are implanted at a dose of 5×10^{12} ions cm^{-2} and an acceleration voltage of 40 keV via the uniform SiO_2 film to form the n^+-type layer 116 serving as a source or drain of the MOSFET in the upper end face of each pillar projection 105. If necessary, phosphorus ions may be implanted at a dose of 3×10^{13} ions cm^{-2} and an acceleration voltage of 100 keV to form an n^-type layer below the layer 116, so that the MOSFET obtains an LDD structure.

An ammonium fluoride solution is used to etch the 10-nm thick SiO_2 film present on the upper end face of the each pillar projection 105, thereby selectively exposing only the upper surface of the projection 105.

A tungsten film W is deposited and patterned to form bit lines 117 connected to the n-type layers 116 and crossing the word lines.

In this manner, according to this example, only the upper surface of each pillar projection 105 can be exposed in a self-alignment manner without a PEP step for a bit line contact.

The DRAM according to this example has the following features.

That is, since an area of the substrate concerning a soft error is reduced, a soft error in a bit line mode can be reduced. Since the memory cells are micropatterned and completely isolated by the insulating layer 102, a soft error in a cell mode is significantly reduced.

In addition, in this example, the bonded wafer formed by direct bonding is used as a starting material, and the oxide film formed by bonding is used as an etching stopper, thereby forming the grooves in longitudinal and transverse directions from the first substrate side by anisotropic etching. Therefore, a groove having a uniform depth can be easily formed at a high density. Also, the insulating layer for isolation can be easily buried while this is very difficult in conventional methods. All the bottom surfaces of the pillar projections 105 are formed on the insulating film 102. Since bonding strength of an interface between the bottom surface of the projection 105 and the insulating film 102 is very high, crystallinity of the projection is good. As a result, a DRAM having good element characteristics can be obtained. That is, only an interface level substantially the same as that produced in an interface between a normal thermal oxide film and silicon is produced in the interface between the MOS capacitor and the insulating film 102. For this reason, leakage between immediately adjacent MOS capacitors can be suppressed, and an electric charge retention property of the DRAM is improved.

The bit line is connected to the source or drain of the MOSFET in a self-alignment manner without a contact hole formation step including photolithography. For this reason, since no alignment margin is required as in the photolithography, the size of the upper end face of the pillar projection 105 is not limited by an alignment margin unlike in conventional structures. As a result, since the pillar projection 105 can be minimized to a patterning limit size, the memory cells can be micropatterned, and a high packing density and a large capacity of the DRAM can be realized.

Since the MOS capacitor is formed by utilizing all the side surfaces at the lower portion of the projection 105, a relatively large storage capacity is assured.

Since the MOSFET is formed by utilizing all the side surfaces at the upper portion of the projection 105, a channel width can be increased. Therefore, the channel length or the thickness of the gate insulating film need not be decreased in order to obtain a large channel conductance. A DRAM having good characteristics can be obtained such that a threshold value variation caused by hot electrons is small.

The step 107 is formed in the middle of the pillar projection 105. The n^--type layer 103 serving as a memory node is formed to have a height substantially equal to that of the step 107 or is located closer to the channel

channel region is very strong, sufficient cutoff characteristics can be obtained even if the substrate potential is floating.

In this modification, the word line at the memory cell portion and the gate electrode 168 at the peripheral circuit are independently formed. The word line 162 and the gate electrode 168, however, may be simultaneously formed. In this manner, manufacturing steps can be simplified.

In the above example, in order to adjust the threshold value of the MOSFET, ion implantation is performed for the entire substrate surface to the depth corresponding to a MOSFET formation region before groove formation, thereby forming the p-type layer. The p-type layer need only be present on at least the side surface portion as the MOSFET formation region of the pillar projection. Therefore, for example, after the pillar projections are formed and the capacitor electrodes are buried, ion implantation may be performed for the side surfaces at the upper portion of each pillar projection to adjust the impurity concentration at only the channel region. In this case, since ion implantation must be performed for the substantially vertical side surfaces, oblique ion implantation including rotation of the wafer is performed. By this ion implantation, an impurity is doped uniformly in the side surfaces. The wafer may be continuously rotated or intermittently rotated every 90°C.

Examples of the bit line material are, in addition to the W film and the Aℓ-Si-Cu film described in the example, another refractory metal such as molybdenum, a refractory metal silicide, or a combination of these metals and a polycrystalline silicon film.

In the above example, the substrates are directly bonded. A substrate layer, however, may be formed to have an insulating layer by an SOI technique using laser annealing. If necessary, an insulating layer may be formed in a lattice manner in the wafer so that all the lower surfaces of the pillar projections are located on the insulating layer.

In the above example, one end of the MOS capacitor is in contact with the insulating layer in the substrate. Only an interface level substantially the same as that produced in an interface between a normal thermal oxide film and silicon is produced in an interface between the MOS capacitor and the insulating layer. For this reason, since leakage between the immediately adjacent MOS capacitors can be suppressed, a electric charge retention property of the DRAM can be improved.

In the above example, the oxide films are formed on the surfaces of the two silicon substrates to be bonded. The oxide film, however, may be formed on the surface of only one of the substrates, e.g., the substrate 101S. In addition, in the above example, the MOSFET is formed on the side wall at the upper portion of each pillar projection. However, the electrode of the MOS capacitor may be buried to the upper portion of the groove to form a frame-like gate electrode of the MOSFET on the upper surface of the pillar projection. Ion implantation for forming a source or drain region may be performed for the upper surface of the pillar projection through an opening formed in the gate electrode. Thereafter, the bit line may be connected to the source or drain region to form the MOSFET on the surface of the pillar projection.

A DRAM according to an embodiment of the present invention will be described below with reference to Figs. 19A to 19C.

Fig. 19A is a plan view showing a six-bit DRAM portion.

An n^--type layer 203 serving as a memory node of a MOS capacitor and a p^--type layer 204 serving as a channel region of a MOSFET are stacked on a silicon oxide film 202 formed on the surface of a p-type silicon substrate 201. A plurality of pillar projections 205a, 205b, 205c and 205d separated by grooves 206 formed in longitudinal and transverse directions in the substrate are arranged in a matrix manner.

Pillar projections 205aa, 205bb and 205cc located at the centers of pillar projection arrays do not form memory cells. A gate electrode material is provided above the upper surface of each of the projections 205aa, 205bb and 205cc with an insulating layer 21 interposed therebetween, and a contact pad is formed thereon.

A MOSFET and a MOS capacitor are formed on side surfaces at upper and lower portions, respectively, of each of pillar projections 205a, 205b, 205c, 205d, 205e and 205f formed at both sides of the projections 205aa, 205bb and 205cc having the contact pads thereon, thereby constituting memory cells.

A step 207 is formed on the side surfaces of each of the projections 205a, 205b, 205c, 205d, 205e and 205f. A portion below a position slightly above the step 207 is the n^--type layer 203 serving as a memory node. A capacitor insulating film 208 is formed on all the side surfaces at the lower portion of each projection 205. A capacitor electrode 209 is buried in the grooves 206. The MOS capacitor is constituted by the layer 203, the film 208 and the electrode 209. A boundary between the n^--type layer 203 and the channel layer 204 is set to substantially coincide with or higher than the position of the step 207. The capacitor electrode is continuously formed as a plate electrode common for all the memory cells and extracted as an electrode at a peripheral portion of the DRAM.

The silicon oxide layer 202 is formed under bottom portions of the grooves 206 and the pillar projections 205. The layer 102 serves as an insulating layer for element isolation and for preventing soft errors caused by α-rays.

Gate electrodes 212a, 212b and 212c are formed on the side surfaces at the upper portions of the projections 205a, 205b and 205c, respectively, with the gate insulating films 211 interposed therebetween. Each gate electrode 212 and the capacitor electrode 209 are vertically stacked in each groove 206 and are isolated by

of the polycrystalline silicon film, a fluid film such as a photoresist is used to flatten the surface. The above structure is obtained by etching the entire surface such that the fluid film and the polycrystalline silicon film are etched at substantially equal etching rates. In this manner, the MOS capacitor is formed on the side surfaces at the lower portion of each projection 205 not covered with the first and second masks 221 and 223.

As shown in Fig. 20E, thermal oxidation is performed in an $O_2 + H_2$ atmosphere at 850°C for about 15 minutes by using the Si_3N_4 films 221 and 223 as masks to form thick SiO_2 film 210 having a thickness of about 80 nm on the surface of the capacitor electrode 209. In this manufacturing step, the capacitor electrode 209 and the gate electrode 212 of each MOSFET are isolated from each other by the thermal oxide film 210. However, a CVD oxide film may be deposited and etched back to the upper portion of the capacitor electrode 209, thereby performing isolation. Since crystal defects caused by a stress produced in a thermal step can be suppressed if CVD is used, a data storage property of each memory cell can be improved.

The Si_3N_4 film 223 as the second mask and the underlying SiO_2 film 222 covering the side surfaces at the upper portion of each projection 205 on which the MOSFET is to be formed are removed. Thermal oxidation is performed in an O2 + HCℓ atmosphere at a temperature of 900°C for about 60 minutes to form the gate insulating film 211 on the side surfaces at the upper portion of the projection 205 to have a thickness of about 20 nm.

Thereafter, as shown in Fig. 20F, a phosphorus-doped second polycrystalline silicon film is deposited to have a thickness of about 250 nm and etched by RIE, thereby forming the gate electrode 212 on the side surfaces at the upper portion of the projection 205. The gate electrode 212 is self-aligned all around the projection 205 without using a mask. The gate electrodes 212 are connected in units of blocks. At the same time, the second polycrystalline silicon film is caused to remain on the upper surfaces of the contact pillar projections 205aa, 205bb and 205cc, thereby constituting the word lines. For this purpose, a photoresist film 224 is formed on regions above the projections 205aa, 205bb and 205cc. If the projections 205 are arranged in a word line direction at an interval smaller than that in a direction perpendicular to the word line direction, connection portions can be self-aligned. In this case, therefore, a photoresist film (mask) need not be formed on regions of the grooves along the word line. Therefore, the photoresist film 224 need only be formed on the upper surface regions of the projections 205aa, 205bb and 205cc, thereby improving patterning precision.

As shown in Fig. 20G, the film 224 is removed, and the surface of the gate electrode 212 is covered with the SiO_2 film 213. A BPSG film 214 is buried in recess portions, and the overall substrate is flattened by annealing. The SiO_2 film 213 may be formed not by thermal oxidation but by CVD.

Thereafter, bit line contacts are formed in the upper surfaces of the projections 205b and 205e. Bit lines 217a and 217b each having a polycide structure consisting of a molybdenum film and a polycrystalline silicon film are connected to the upper surfaces of the projections 205b and 205e. That is, a 50-nm thick polycrystalline silicon film 217aa is deposited on the exposed upper surface of each of the projections 205b and 205e, and arsenic ions are implanted in the film 217aa at an acceleration voltage of 60 keV and a dose of 5×10^{15} ions/cm^2. A 20-nm thick molybdenum silicide film 217bb is deposited on the film 217aa. The films 217aa and 217bb are patterned by normal photolithography. At this time, arsenic is diffused from the polycrystalline silicon film 217aa in which arsenic is doped at a high concentration into the upper surface of the projection 205 to form an n^+-type layer 218 in the n^--type layer 231 constituting the source or drain. In this manufacturing step, contact resistances between the layers 231 in the upper surfaces of the projections 205b and 205e and the bit lines 217a and 217b can be reduced. Since the bit line has a polycide structure, an electrical resistance of wiring itself is low.

As shown in Fig. 20H, the surface of each bit line 217 is oxidized to form a 50-nm thick oxide film, and a BPSG film 219 is deposited on the entire surface to have a thickness of about 800 nm and flattened by annealing. Thereafter, a contact hole is formed in the gate electrode 212b on the upper surface of the projection 205bb by normal photolithography, thereby forming each word shunt line 220 consisting of an aluminum layer.

The DRAM according to this embodiment has the following features.

The gate electrodes 212 constituting the word lines need not be extended from the end portion of a memory cell array over the grooves. Each of the contact pillar projections 205aa, 205bb and 205cc is formed in each block, and the word shunt line 220 is extracted from the contact pad P on the upper surface of each pillar projection. Therefore, even if a gate electrode material 250 remains on side walls of a step present at the end portion of a memory cell array (see Fig. 19A), the word shunt lines 220a, 220b and 220c are not short-circuited with each other. As a result, the yield of the DRAM can be improved.

Since the contact pad P is formed on the insulating film used as a mask for formation of the grooves 206, no gate breakdown occurs even if a high electric field is applied.

In this embodiment, the word line is not extracted from the end portion of each block but from the center thereof. In addition, the word shunt line 220 consisting of an aluminum layer is formed after the surface of the semiconductor structure is flattened in units of blocks. Therefore, a word line resistance is decreased as a whole to increase an operation speed.

Furthermore, since an etching step for preventing short-circuiting between the gate electrodes need not

ly bonded. However, a substrate layer having an insulating layer may be formed by an SOI technique using, i.e., laser annealing. If necessary, the insulating layer may be formed on the wafer in a matrix manner so that all the lower surfaces of the pillar projections are located on the insulating layer. In addition, in order to isolate MOS capacitors of adjacent bits, the insulating layer may be formed on only regions close to the pillar projections.

In this embodiment, one end of each MOS capacitor is in contact with the insulating layer in the substrate. Only an interface level substantially the same as that produced in an interface between a normal thermal oxide film and silicon is produced in an interface between the MOS capacitor and the insulating layer. For this reason, leakage between MOS capacitors very close to each other can be suppressed. As a result, an electric charge retention property of the DRAM can be improved.

In the above embodiment, the oxide films are formed on the surfaces of both the silicon substrates upon bonding. The oxide film, however, may be formed on only one of the substrates, e.g., the substrate 201S. In the above embodiment, the MOSFET is formed on the side walls at the upper portion of each pillar projection. The electrode of the MOS capacitor, however, may be buried in the upper portion of the groove to form the frame-like gate electrode of the MOSFET on the upper surface of the pillar projection. Ion implantation is then performed to form a source or drain region in the upper surface of the pillar projection through an opening formed in the gate electrode. Thereafter, a bit line is connected to the source or drain region, thereby forming the MOSFET on the upper portion of the pillar projection.

Claims

1. A dynamic RAM comprising:

a semiconductor substrate;
a plurality of semiconductor pillar projections separated by grooves formed in longitudinal and transverse directions in said semiconductor substrate, said semiconductor pillar projections being arranged in a matrix manner;
a plurality of MOS capacitors formed on side surfaces at a lower portion of each of said semiconductor pillar projections, said each MOS capacitor including,
a memory node formed in side surface at the lower portion of each semiconductor pillar projection,
a capacitor insulating film formed on the side surface at the lower portion of each semiconductor pillar projection, and
a capacitor electrode formed on said capacitor insulating film;
a plurality of MOSFETs formed on side surfaces at an upper portion of each semiconductor pillar projection, said each MOSFET including,
a channel region formed at least on the side surface at the upper portion of each semiconductor pillar projection,
source and drain regions formed above and below said channel region to sandwich said channel region,
a gate insulating film formed on the side surface at the upper portion of each semiconductor pillar projection in which said channel region is formed, and
a gate electrode formed on said gate insulating film;
a plurality of bit line contacts each contact formed on an upper surface of a corresponding semiconductor pillar projection; and
a plurality of bit lines each bit line connected to associated bit line contacts;

characterized in that said plurality of semiconductor pillar projections is divided into a plurality of blocks, each block having at least one contact semiconductor pillar projection comprising a first insulating layer which is thicker than said gate insulating film of said MOSFET and is formed on an upper surface of said contact semiconductor pillar projection, and a word line contact pad formed on said first insulating layer, said contact pad being electrically connected to said gate electrode of memory cells in each block.

2. A dynamic RAM according to claim 1, further characterized in that said contact pillar projection is arranged close to a center of each block.

3. A dynamic RAM according to claim 1, further characterized in that said semiconductor pillar projection is formed on a second insulating layer buried in said semiconductor substrate.

4. A dynamic RAM according to claim 3, further characterized in that said substrate comprises two semiconductor substrates each having an insulating film thereon, said insulating films being bonded together.

5. A dynamic RAM according to claim 1, further characterized in that said semiconductor pillar projections have upper and lower portions which define a step therebetween.

6. A dynamic RAM according to claim 5, further characterized in that said memory node includes a diffusion layer formed on the side surface at the lower portion of each semiconductor pillar projection, said diffusion layer being deep enough to reach at least

Revendications

1. RAM dynamique comprenant:

un substrat semiconducteur:
plusieurs saillies sous forme de pilier semiconducteur séparées par des gorges formées dans les directions longitudinales et transversales dans ledit substrat semiconducteur. lesdites saillies en forme de pilier semiconducteur étant disposées en matrice;
plusieurs condensateurs MOS formés sur les surfaces latérales au niveau de la partie inférieure de chacune desdites saillies en forme de pilier semiconducteur, chacune desdits condensateurs MOS englobant:
un noeud de mémoire formé dans la surface latérale au niveau de la partie inférieure de chaque saillie en forme de pilier semiconducteur,
un film isolant de condensateur formé sur la surface latérale au niveau de la partie inférieure de chaque saillie en forme de pilier semiconducteur, et
une électrode de condensateur formée sur ledit film isolant du condensateur:
plusieurs MOSFET formés sur les surfaces latérales au niveau d'une partie supérieure de chaque saillie en forme de pilier semiconducteur, chacun desdits MOSFET englobant,
une région de canal formée au moins sur la surface latérale au niveau de la partie supérieure de chaque saillie en forme de pilier semiconducteur,
des régions de source et de drain formées au-dessus et au-dessous de ladite région de canal pour entourer en sandwich ladite région de canal,
un film d'isolation de grille formé sur la surface latérale au niveau de la partie supérieure de chaque saillie en forme de pilier semiconducteur dans laquelle est formée ladite région de canal, et
une électrode de grille formée sur ledit film d'isolation de grille;
plusieurs contacts de lignes de bit, chaque contact étant formé sur une surface supérieure d'une saillie en forme de pilier semiconducteur correspondante; et
plusieurs lignes de bit, chaque ligne de bit étant connectée à des contacts de ligne de bit associés;

caractérisé en ce que lesdites plusieurs saillies en forme de pilier semiconducteur sont divisées en plusieurs blocs, chaque bloc comportant au moins une saillie en forme de pilier semiconducteur de contact, comprenant une première couche isolante, plus épaisse que ledit film d'isolation de grille dudit MOSFET et formée sur une surface supérieure de ladite saillie en forme de pilier semiconducteur de contact, et un plot de contact de ligne de mot formé sur ladite première couche isolante, ledit plot de contact étant connecté électriquement à ladite électrode de grille des cellules de mémoire dans chaque bloc.

2. RAM dynamique selon la revendication 1, caractérisée en outre en ce que ladite saillie en forme de pilier de contact est agencée près d'un centre de chaque bloc.

3. RAM dynamique selon la revendication 1, caractérisée en outre en ce que ladite saillie en forme de pilier semiconducteur est formée sur une deuxième couche isolante enterrée dans ledit substrat semiconducteur.

4. RAM dynamique selon la revendication 3, caractérisée en outre en ce que ledit substrat comprend deux substrats semiconducteurs, comportant chacun un film isolant, lesdits films isolants étant assemblés.

5. RAM dynamique selon la revendication 1, caractérisée en outre en ce que lesdites saillies en forme de pilier semiconducteur comportent des parties supérieure et inférieure définissant un palier entre elles.

6. RAM dynamique selon la revendication 5. caractérisée en outre en ce que ledit noeud de mémoire englobe une couche de diffusion formée sur la surface latérale au niveau de la partie inférieure de chaque saillie en forme de pilier semiconducteur, ladite couche de diffusion étant suffisamment profonde pour atteindre au moins les surfaces latérales au niveau de la partie supérieure de chaque saillie en forme de pilier semiconducteur.

7. RAM dynamique selon la revendication 1, caractérisée par une couche isolante enterrée dans ledit substrat semiconducteur, lesdites saillies en forme de pilier semiconducteur étant formées sur une partie dudit substrat semiconducteur agencé sur ladite couche isolante.

8. RAM dynamique selon la revendication 7, caractérisée en ce que ledit substrat comprend deux substrats semiconducteurs comportant des films isolants, lesdits films isolants étant assemblés.

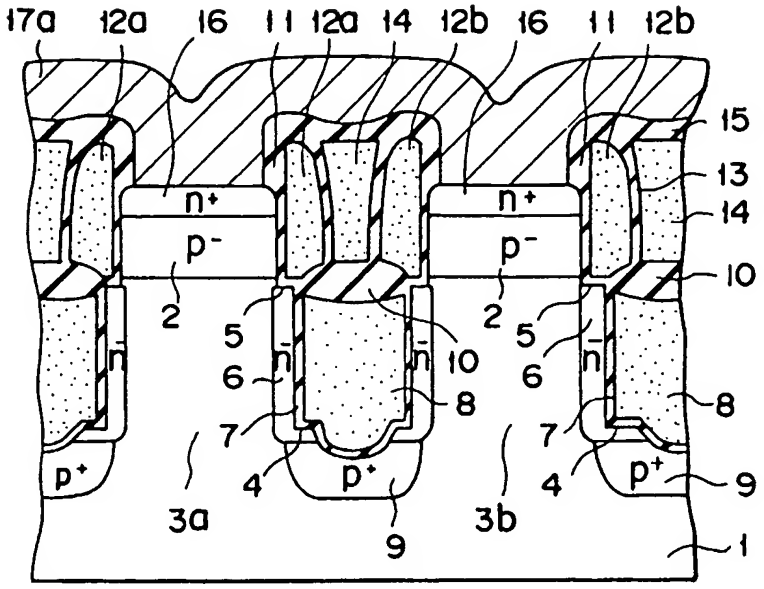
17a
12a
16
11
12a
14
12b
16
11
12b
15
13
14
10
n+
p-
2
5
6
7
4
p+
3a
9
3b
1
8

FIG. 2A

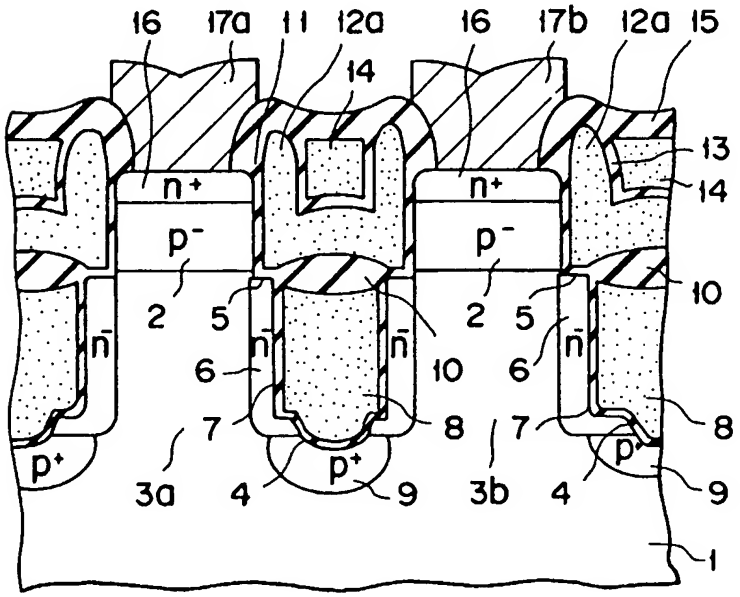
16
17a
11
12a
14
16
17b
12a
15
13
14
10
n+
p-
2
5
6
7
4
p+
3a
9
3b
1
8

FIG. 2B

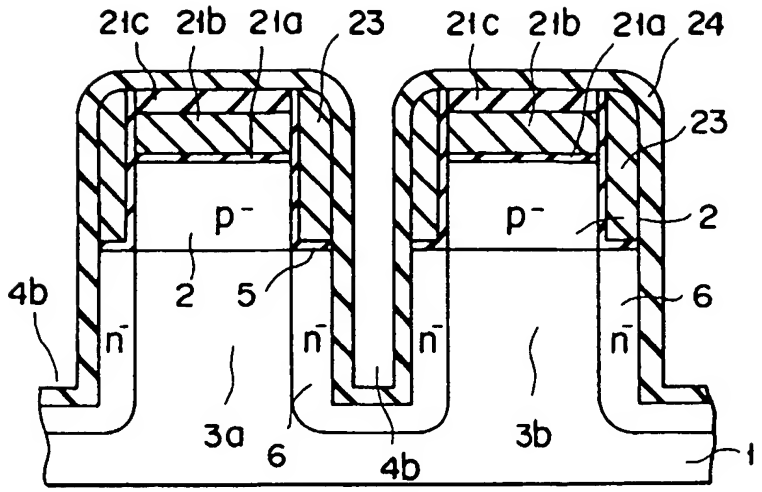
21c
21b
21a
23
21c
21b
21a
24
23
p⁻
p⁻
2
4b
2
5
6
n⁻
n⁻
n⁻
n⁻
3a
6
4b
3b
1

FIG. 3C

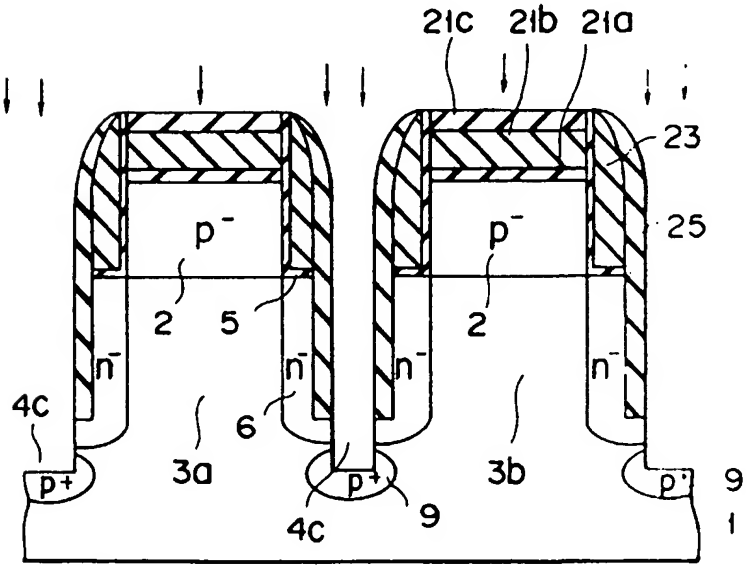
21c
21b
21a
23
25
p⁻
p⁻
2
5
2
n⁻
n⁻
n⁻
n⁻
4c
6
3a
3b
p+
p+
p+
9
4c
9
1

FIG. 3D

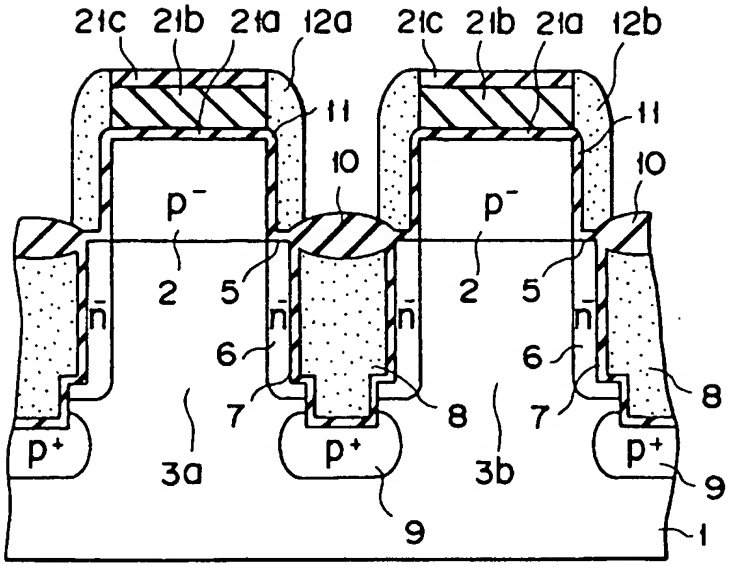
21c
21b
21a
12a
21c
21b
21a
12b
11
11
10
10
p⁻
p⁻
2
5
2
5
n⁻
n⁻
n⁻
n⁻
6
6
7
8
7
8
p⁺
p⁺
p⁺
3a
3b
9
9
1

FIG. 3G

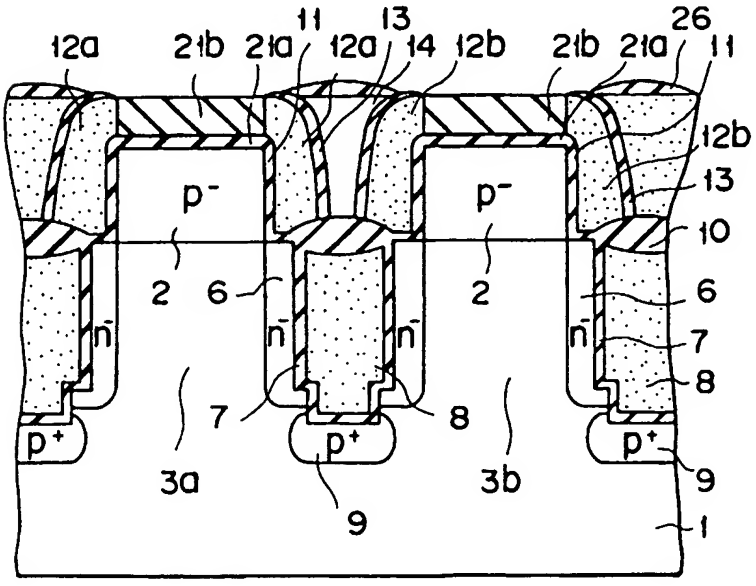
12a
21b
21a
11
12a
13
14
12b
21b
21a
26
11
12b
13
p⁻
p⁻
10
2
6
2
6
n⁻
n⁻
n⁻
n⁻
7
8
7
8
p⁺
p⁺
p⁺
3a
3b
9
9
1

FIG. 3H

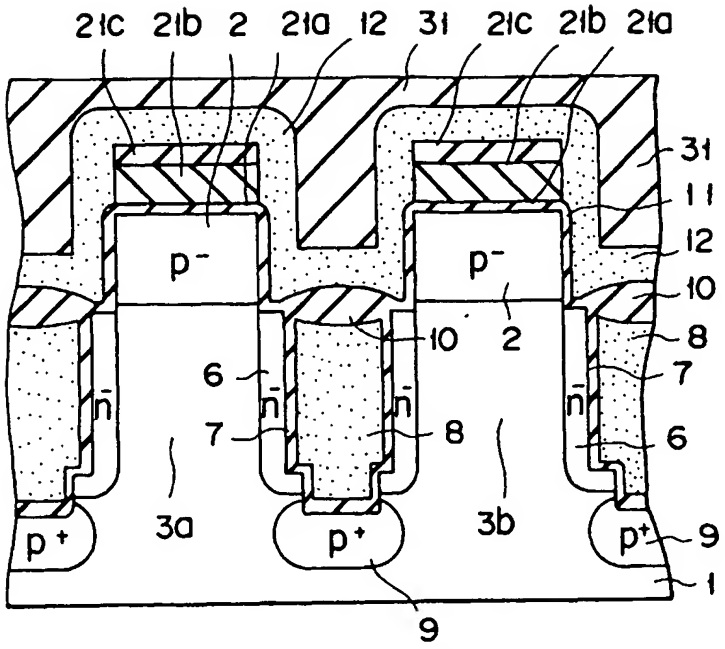
21c
21b
2
21a
12
31
21c
21b
21a
31
11
12
10
8
7
6
p⁻
p⁻
10
2
6
7
8
n⁻
n⁻
n⁻
n⁻
3a
3b
p⁺
p⁺
p⁺
9
1
9

FIG. 5A

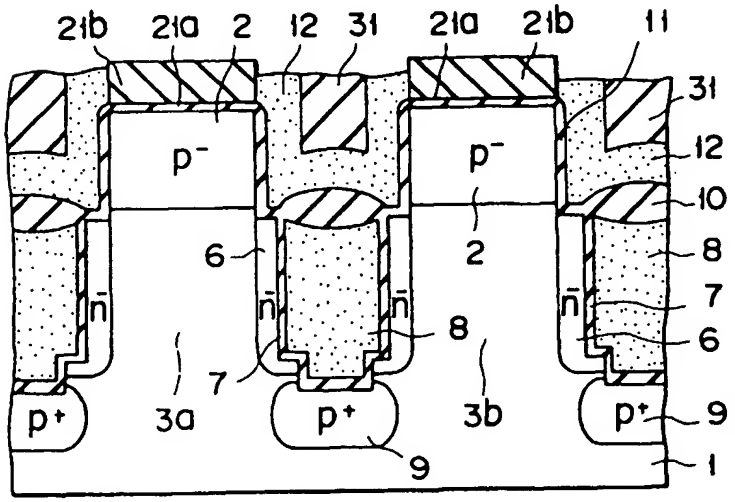
21b
21a
2
12
31
21a
21b
11
31
12
10
8
7
6
p⁻
p⁻
6
2
n⁻
n⁻
n⁻
n⁻
8
7
3a
3b
p⁺
p⁺
p⁺
9
1
9

FIG. 5B

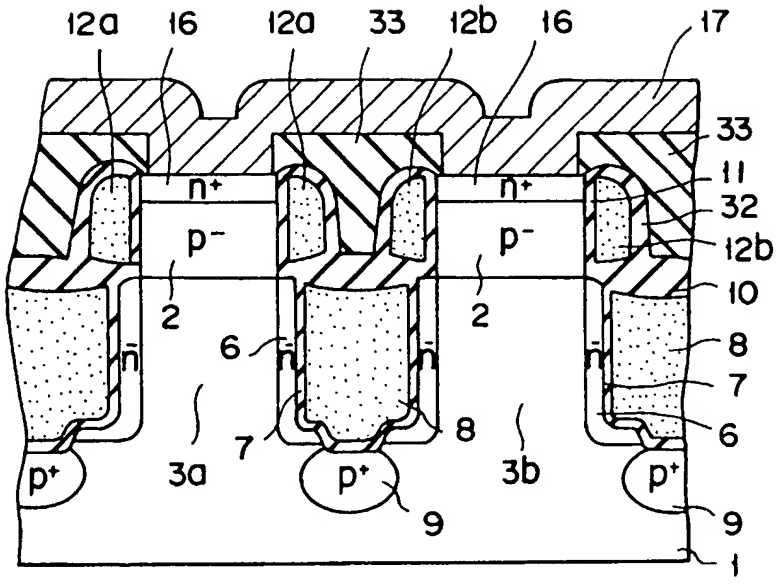
12a
16
12a
33
12b
16
17
33
11
32
12b
10
8
7
6
n+
n+
p-
p-
2
2
6
n-
n-
n-
7
8
3a
3b
p+
p+
p+
9
9
1

FIG. 5E

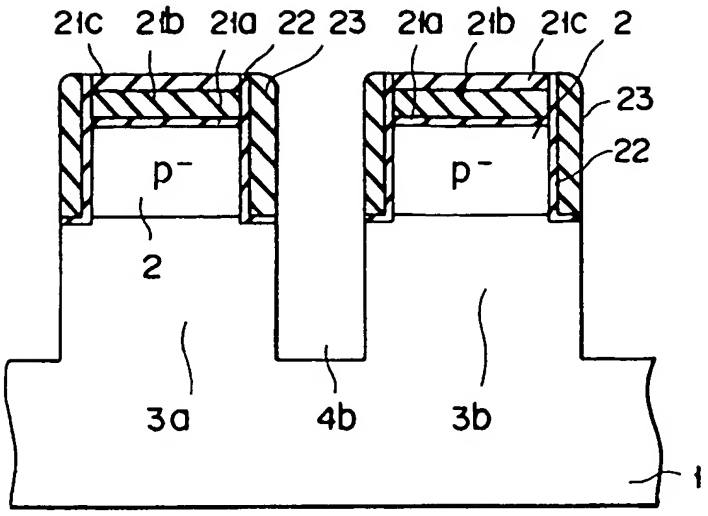
21c
21b
21a
22
23
21a
21b
21c
2
23
22
p⁻
p⁻
2
3a
4b
3b
1

FIG. 7A

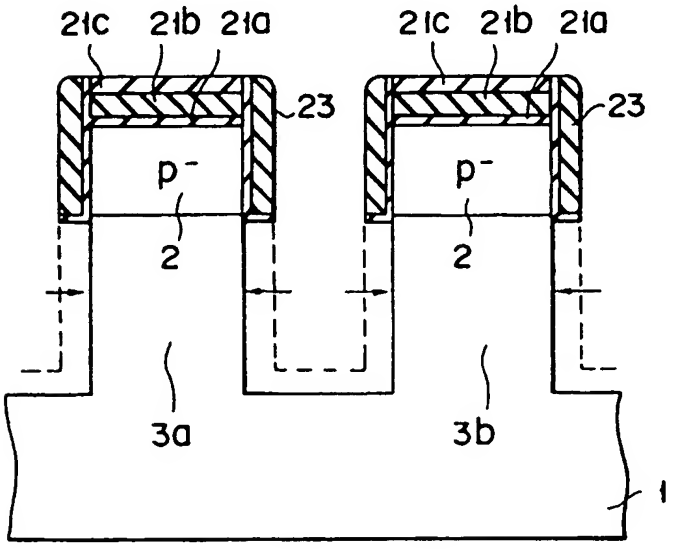
21c
21b
21a
21c
21b
21a
23
23
p⁻
p⁻
2
2
3a
3b
1

FIG. 7B

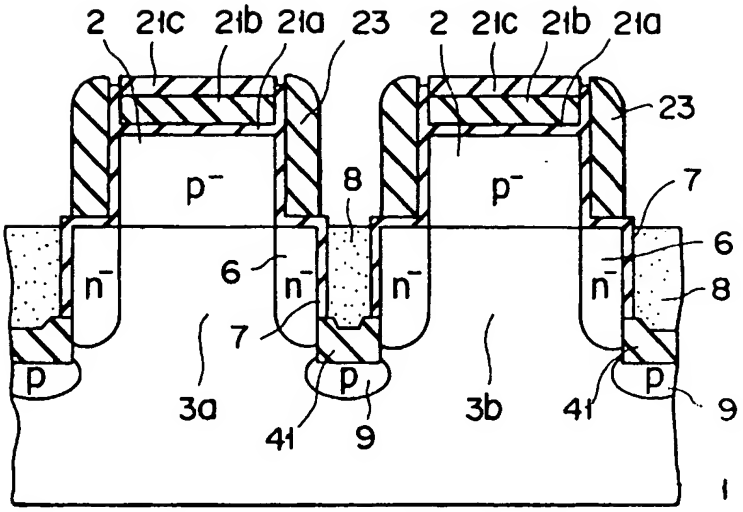
2
21c
21b
21a
23
2
21c
21b
21a
23
p⁻
8
p⁻
7
6
n⁻
6
n⁻
n⁻
n⁻
8
7
p
p
p
3a
41
9
3b
41
9
1

FIG. 8C

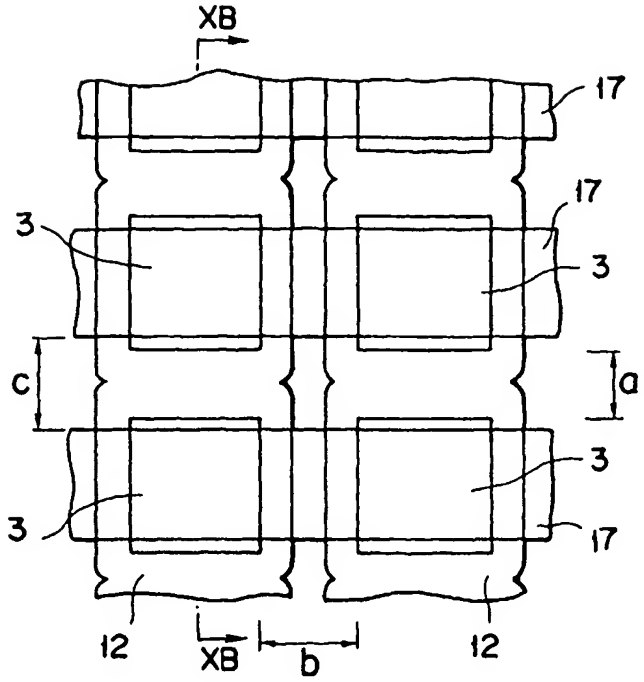

FIG. 10A

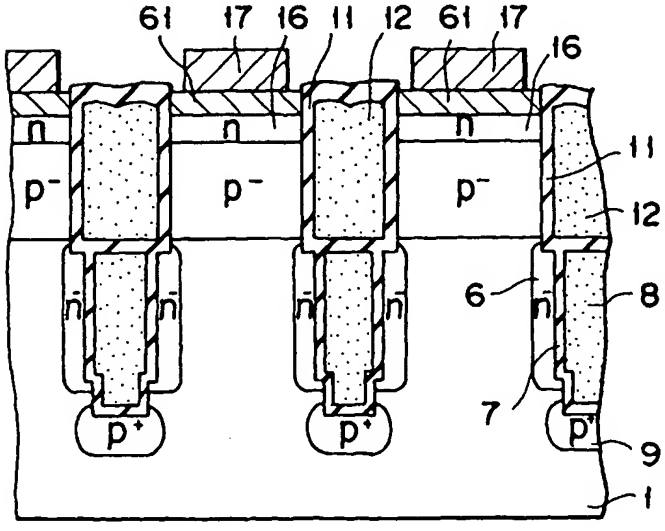

FIG. 10B

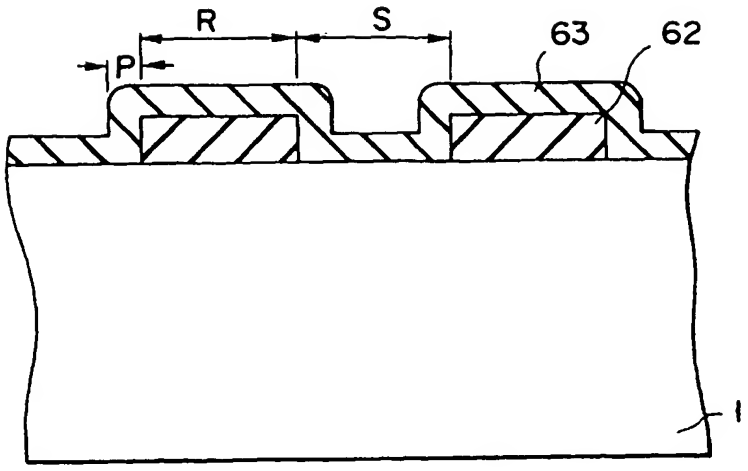

FIG. 12A

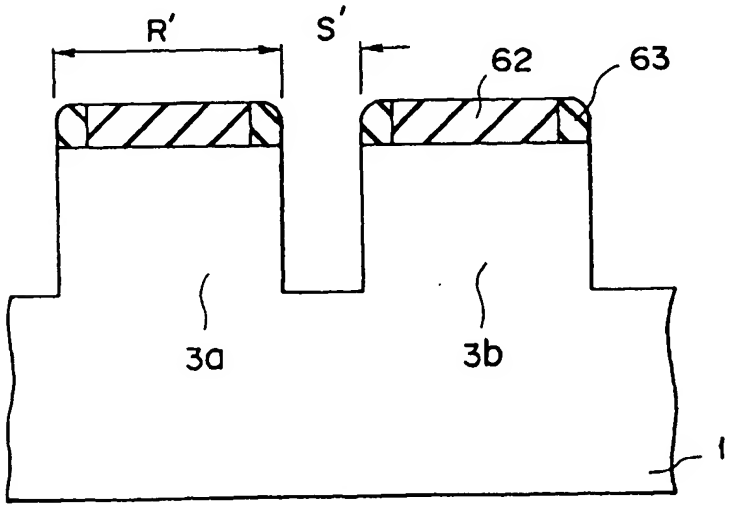

FIG. 12B

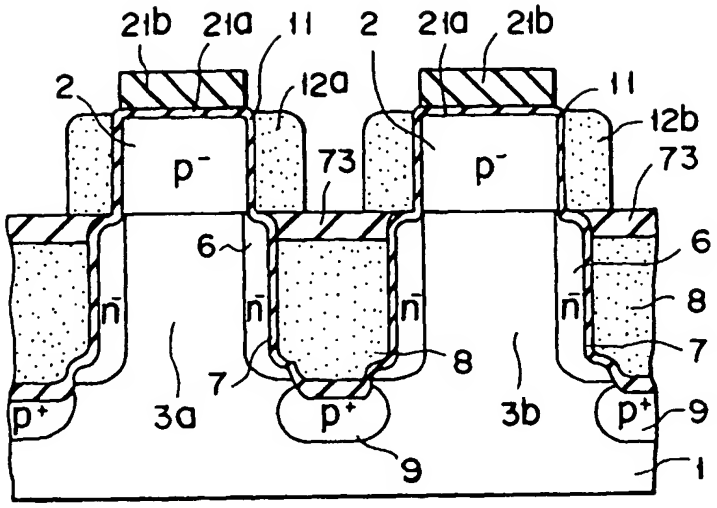

FIG. 13C

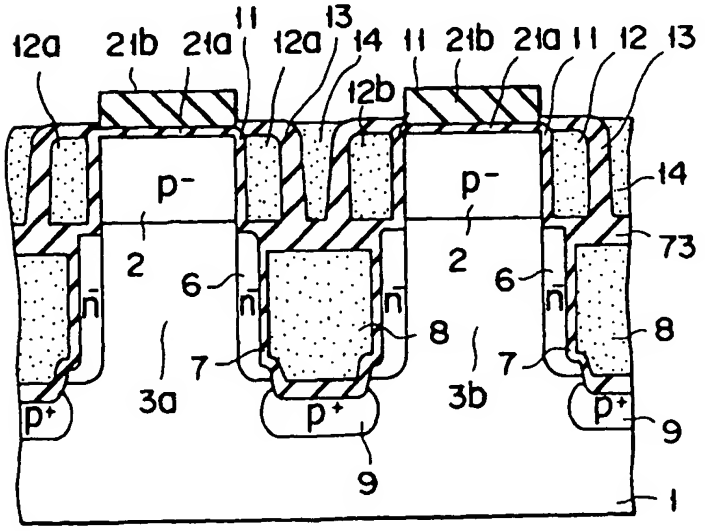

FIG. 13D

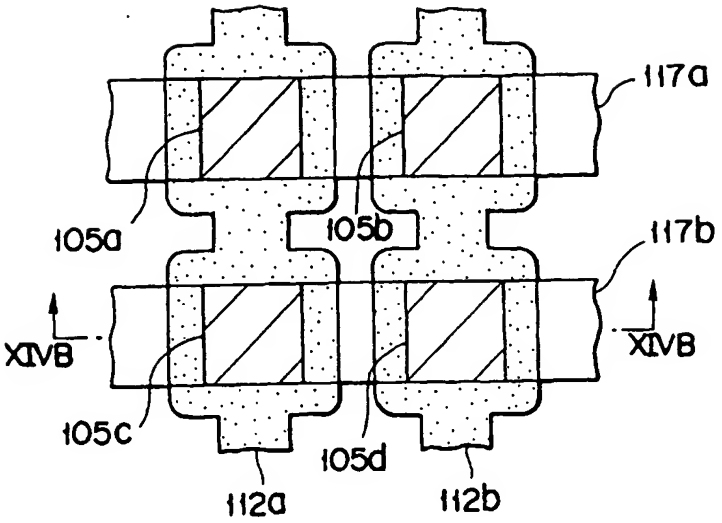

FIG. 14A

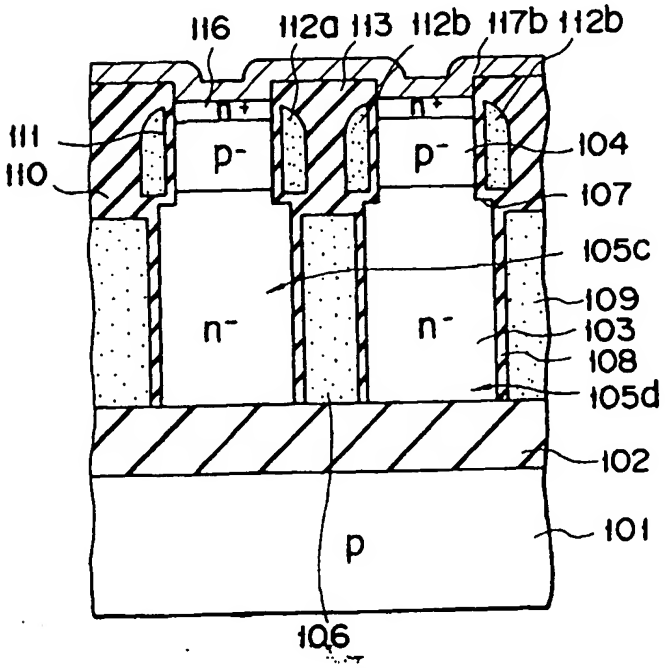

FIG. 14B

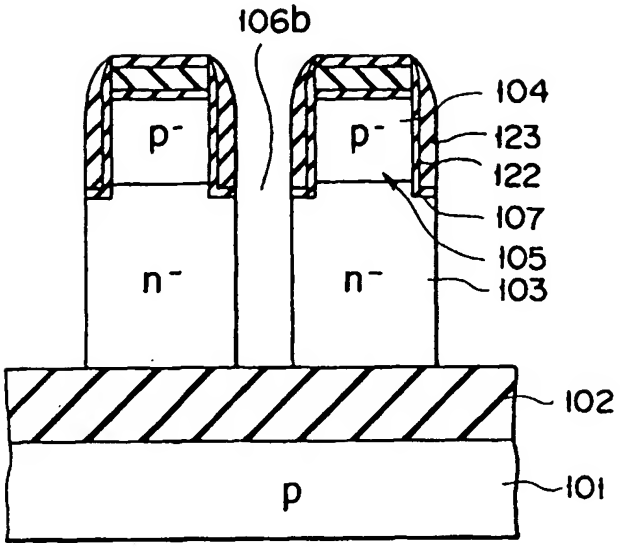

FIG. 15C

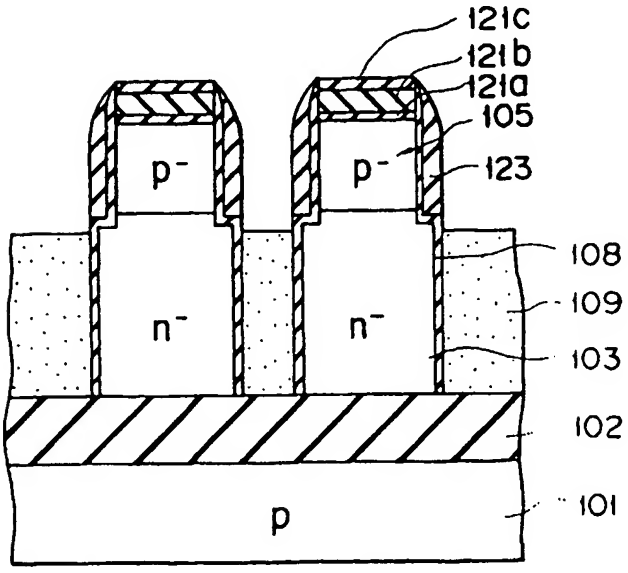

FIG. 15D

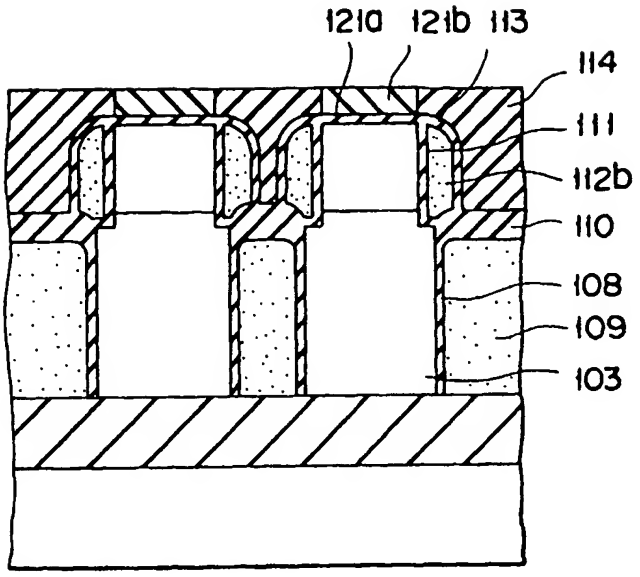

FIG. 15G

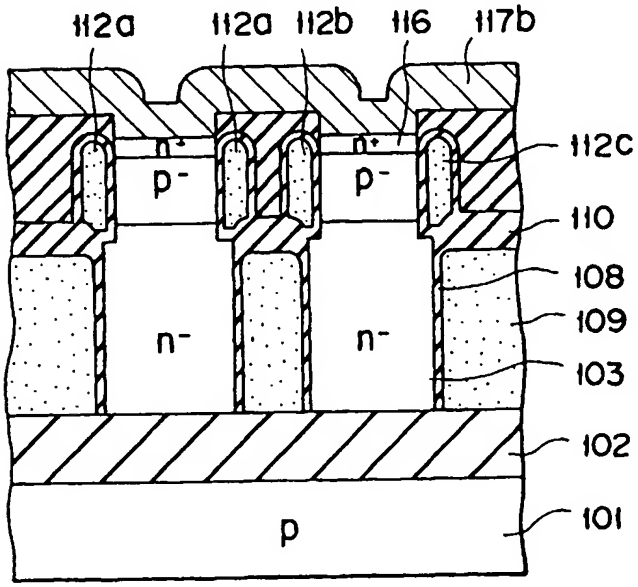

FIG. 15H

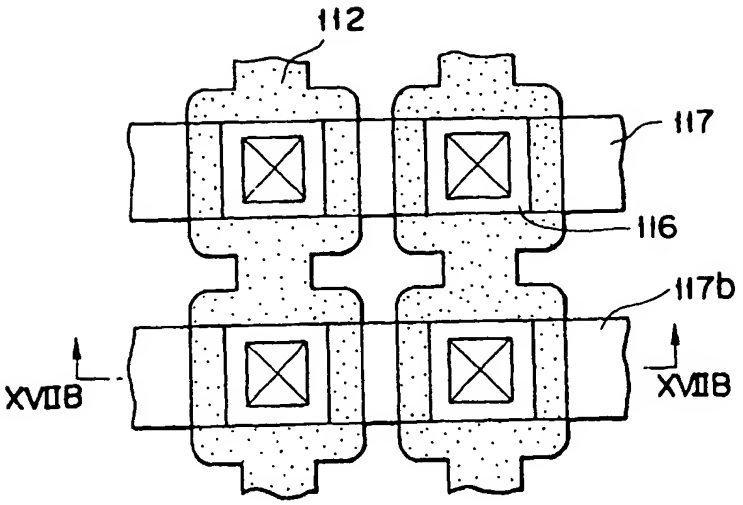

FIG. 17A

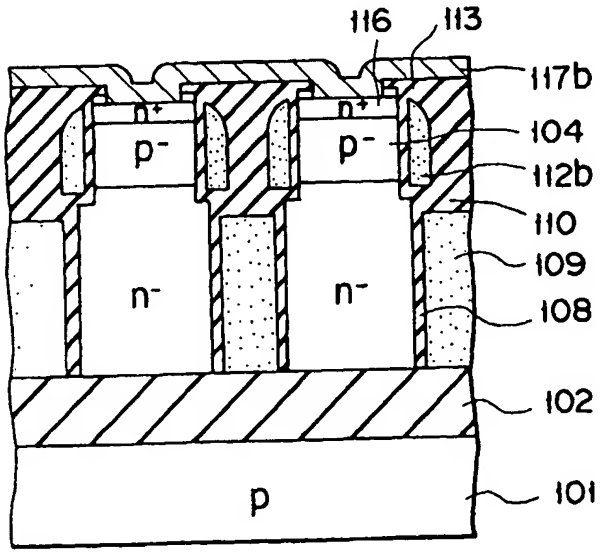

FIG. 17B

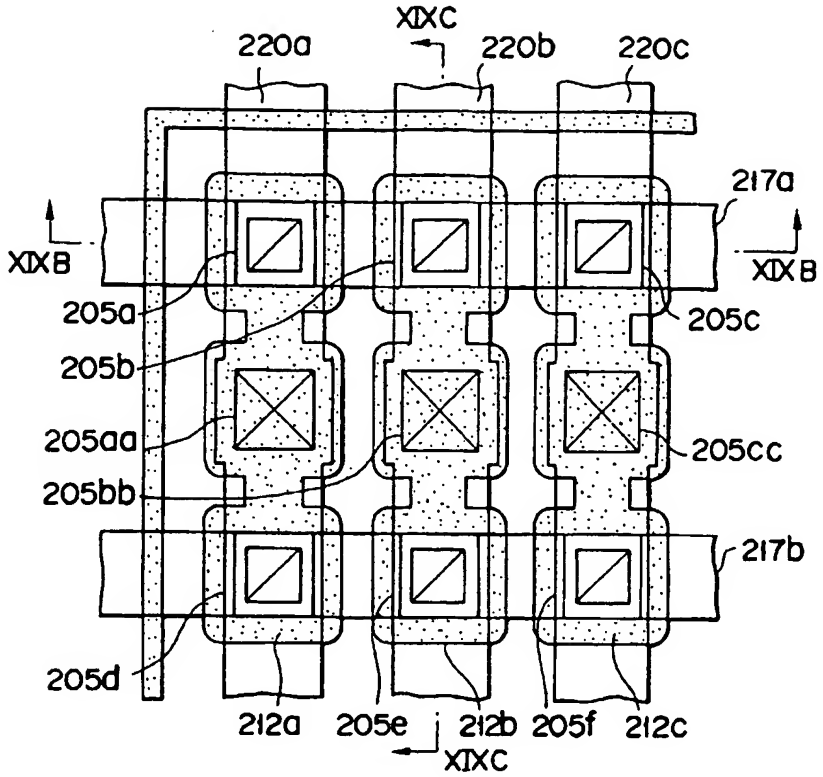

FIG. 19A

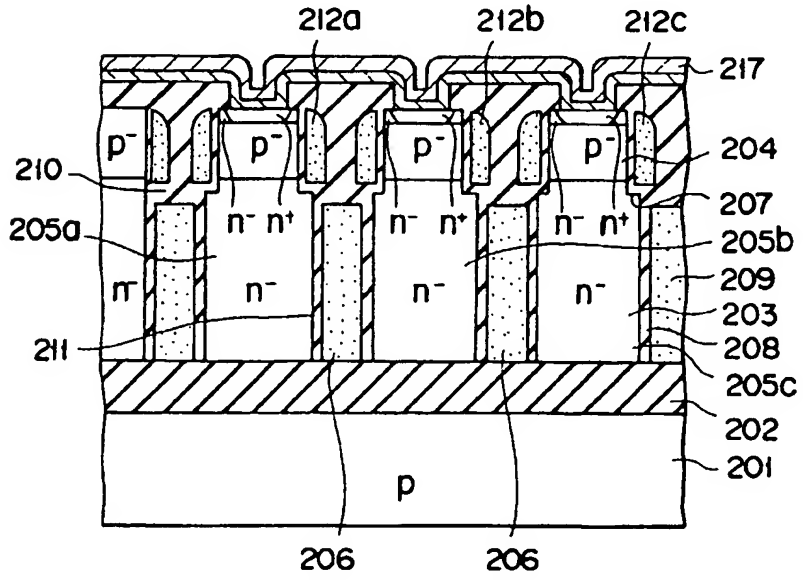

FIG. 19B

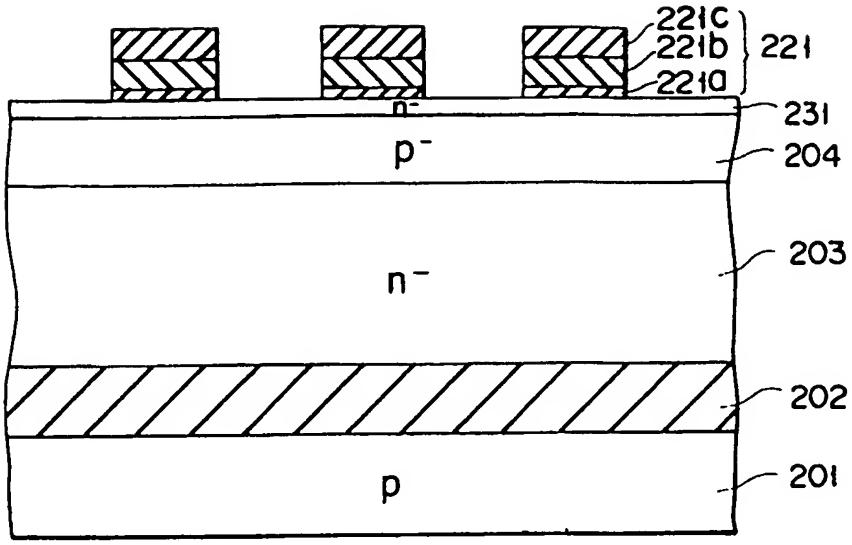

FIG. 20A

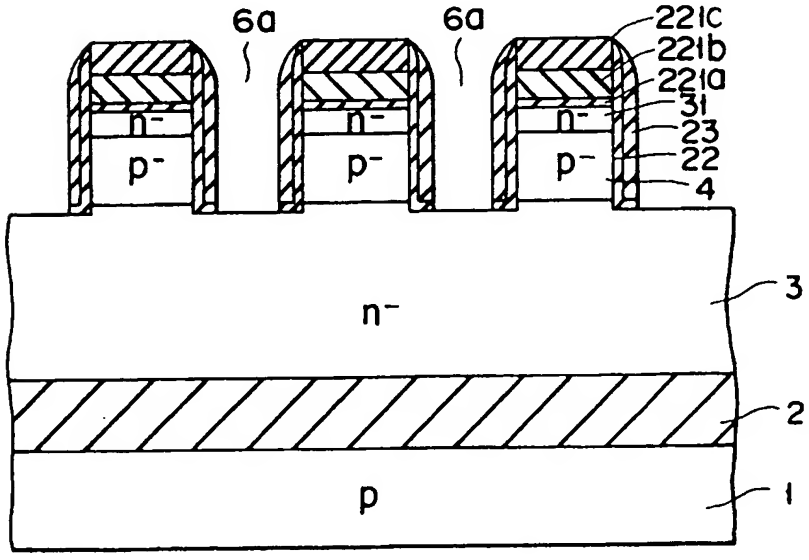

FIG. 20B

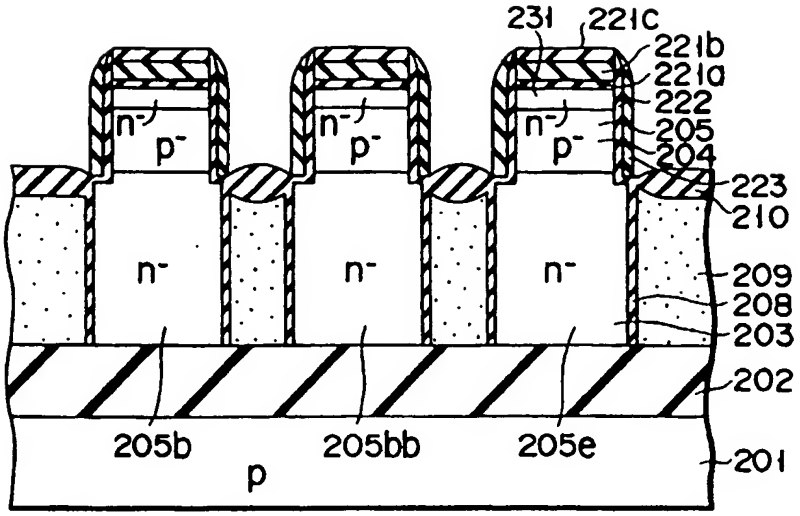

FIG. 20E

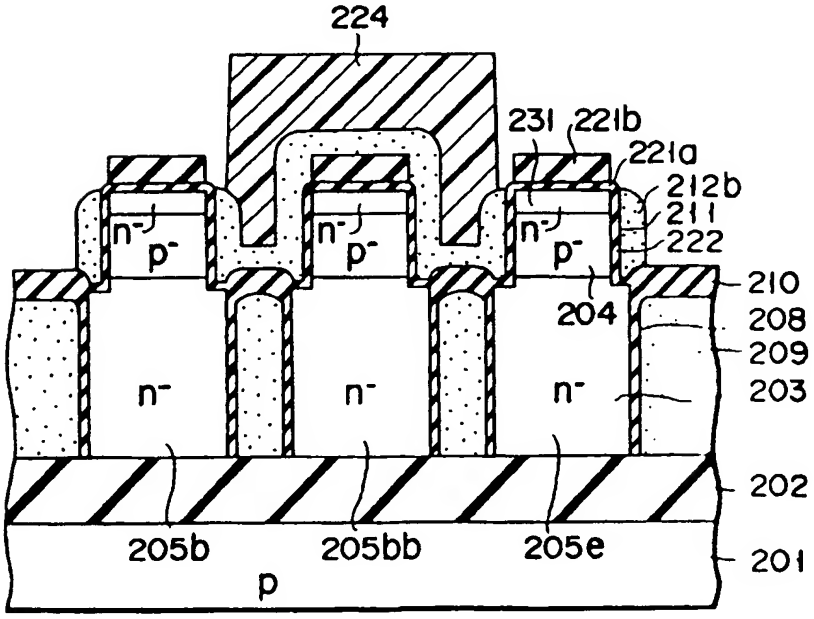

FIG. 20F

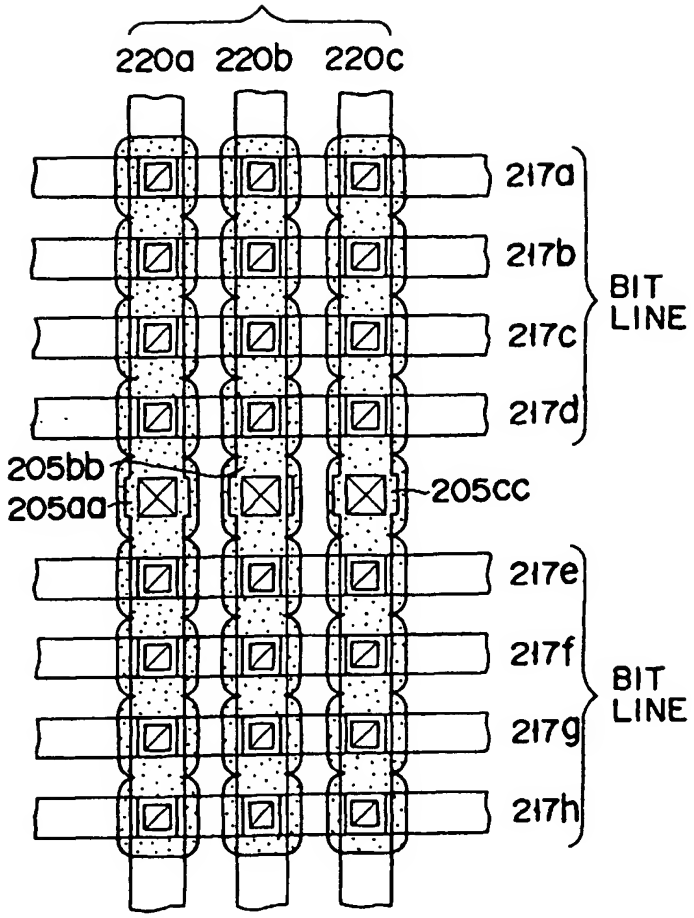
220a
220b
220c
217a
217b
217c
217d
BIT LINE
205bb
205aa
205cc
217e
217f
217g
217h
BIT LINE

FIG. 21

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